What is claimed is:

Sub B1

1. A signal processing circuit for transmitting data to be transmitted as a packet data to a serial interface bus in a predetermined time cycle, comprising:

a cipher processing circuit for enciphering the data to be transmitted by a predetermined cipher mode and

a transmission circuit for adding the enciphering information to the data enciphered in the cipher processing circuit, transmitting the result to the serial interface bus, confirming the continuity of the cipher mode by the enciphering information when transmitting a plurality of packets, and transmitting the data enciphered by a different cipher mode to the serial interface bus as packet data in the other cycle when a discontinuity is confirmed.

2. A signal processing circuit as set forth in claim 1, wherein the transmission circuit sets the enciphering information in a predetermined region of a header of the packet.

3. A signal processing circuit for transmitting data to be transmitted as packet data to a serial interface bus in a predetermined time cycle, comprising:

a holding means in which information of at least one cipher mode is set;

a control means for specifying a mode to encipher transmission data;

a cipher processing circuit including a cipher mode selection circuit for selecting cipher mode information specified by the control means from the holding means and a cipher engine circuit for enciphering the data to be transmitted in the cipher mode selected in the cipher mode selection circuit and outputting the enciphered data;

a transmission circuit for adding the enciphering information to the enciphered data in the cipher processing circuit, transmitting the result to the serial interface bus, confirming the continuity of the cipher mode by the enciphering information when transmitting a plurality of packets, and transmitting the data enciphered by a different cipher mode to the serial interface bus as packet data in the other cycle when a discontinuity is confirmed.

4. A signal processing circuit as set forth in claim 3, wherein the transmission circuit sets the enciphering information in a predetermined region of a header of the packet.

5. A signal processing circuit for transmitting data to be transmitted as packet data to a serial interface bus in a predetermined time cycle, comprising:

a storing means;

a holding means in which information of at least one cipher mode is set;

a control means for specifying a mode to encipher the transmission data;

a cipher processing circuit including a cipher mode selection circuit for selecting cipher mode information specified by the control means from the holding means and a cipher engine circuit for enciphering the data to be transmitted in the cipher mode selected in the cipher mode selection circuit and outputting the enciphered data;

a first transmission circuit for generating time information to output received data on a receiving side to an application side, adding to the time information the enciphering information, and storing the result in the storing means along with the enciphered data; and

a second transmission circuit for reading enciphered data to which has been added time information and enciphering information stored in the storing means, generating packet data in a predetermined format, setting the enciphering information in the packet header, and transmitting the result to the serial interface bus and, when transmitting a plurality of packets, confirming

continuity of the cipher mode from the enciphering information, stopping the transmission when confirming a discontinuity even if there is room in a band enabling transmission in the predetermined time cycle, and transmitting the data enciphered by a different cipher mode to the serial interface bus as packet data in the next cycle.

6. A signal processing circuit for transmitting data to be transmitted as packet data to a serial interface bus in a predetermined time cycle, wherein the enciphered packet data to be transmitted in the serial interface bus in a predetermined cycle is received and output to the application side, comprising:

a cipher processing circuit for enciphering the data to be transmitted by a predetermined cipher mode at the time of transmission and deciphering the received enciphered data based on the enciphering information included in the received packet data at the time of reception and

a transmission circuit for adding the enciphering information to the enciphered data in the cipher processing circuit, transmitting the result to the serial interface bus, confirming the continuity of the cipher mode by the enciphering information when transmitting a plurality of packets, and transmitting the

data enciphered by a different cipher mode to the serial interface bus as packet data in the other cycle when a discontinuity is confirmed.

7. A signal processing circuit as set forth in claim 6, wherein the transmission circuit sets the enciphering information in a predetermined region of a header of the packet.

8. A signal processing circuit for transmitting data to be transmitted as packet data to a serial interface bus in a predetermined time cycle, wherein the enciphered packet data to be transmitted in the serial interface bus in a predetermined cycle is received and output to the application side, comprising:

a first storing means;

a second storing means;

a holding means in which information of at least one cipher mode is set;

a control means for specifying a mode encipher the transmission data;

a first reception circuit for storing time information, enciphered data and the enciphering information from the received packet data in the first storing means;

a second reception circuit for outputting the

enciphering information and the enciphered data stored in the first storing means and indicating a time to be output the received data to an application side based on the time information,

a cipher processing circuit including a cipher mode detection circuit for detecting a cipher mode used for enciphering data by the enciphering information from the second reception circuit, a cipher mode selection circuit for selecting cipher mode information specification by the control means at the time of transmission and selecting the cipher mode information detected by the cipher mode detection circuit from the information set in the holding means at the time of reception, and a cipher engine circuit for enciphering the data to be transmitted in the cipher mode selected in the cipher mode selection circuit and outputting the enciphered data at the time of transmission and deciphering the received data in the cipher mode selected in the cipher mode selection circuit at the time of reception,

a first transmission circuit for generating time information to output received data on a receiving side to an application side, adding to the time information the enciphering information, and storing the result in the second storing means along with the

enciphered data, and

a second transmission circuit for reading enciphered data to which has been added time information and enciphering information stored in the second storing means, generating packet data in a predetermined format, setting the enciphering information in the packet header and transmitting the result to the serial interface bus and, when transmitting a plurality of packets, confirming the continuity of the cipher mode from the enciphering information, stopping the transmission when confirming a discontinuity even if there is room in a band enabling transmission in the predetermined time cycle, and transmitting the data enciphered by a different cipher mode to the serial interface bus as packet data in the next cycle.